CMOS IMAGE SENSORS

An introduction to the technology, design, and performance limits, presenting recent developments and future directions.

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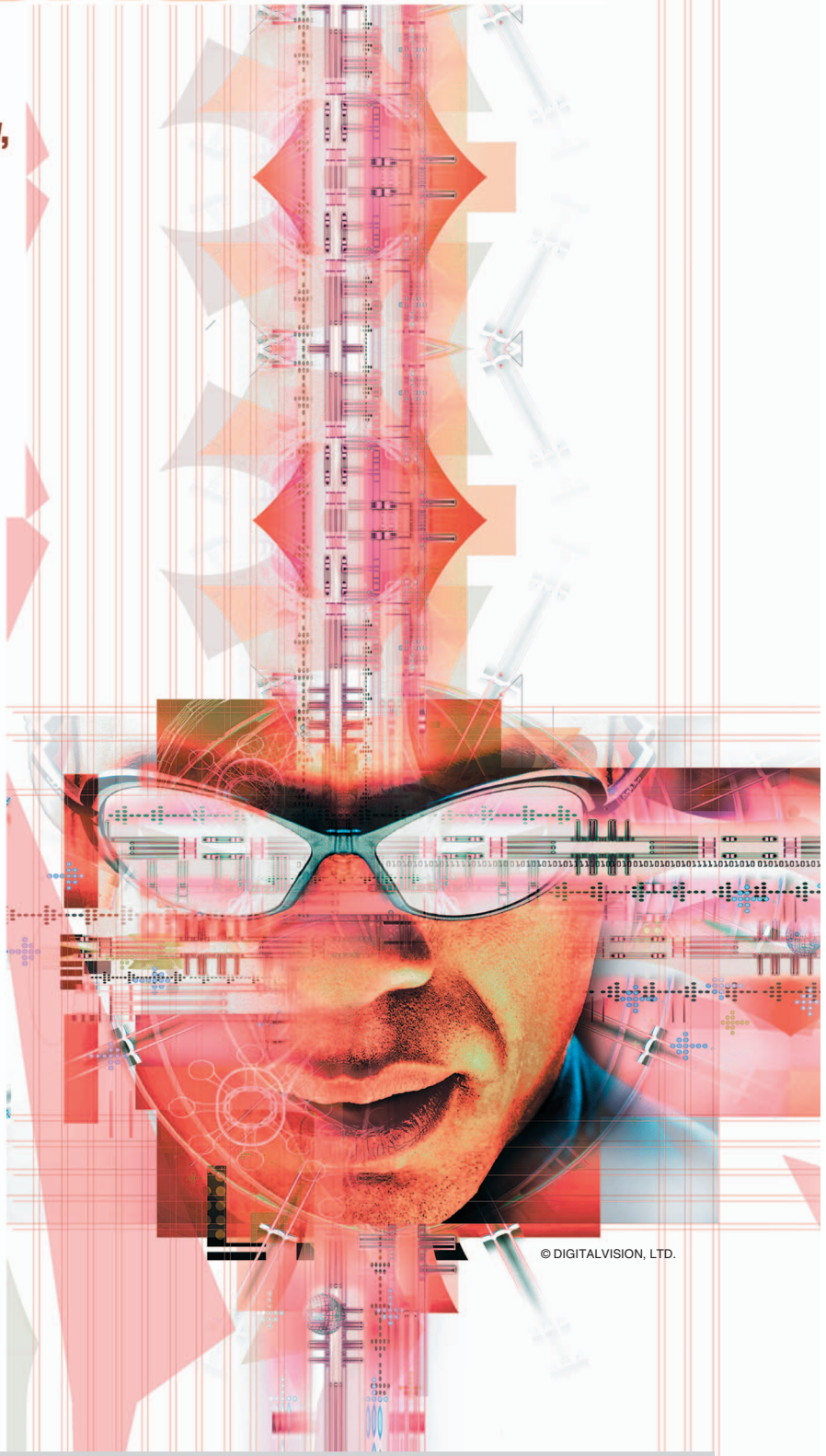

The market for solid-state image sensors has been experiencing explosive growth in recent years due to the increasing demands of mobile imaging, digital still and video cameras, Internet-based video conferencing, surveillance, and biometrics. With over 230 million parts shipped in 2004 and an estimated annual growth rate of over 28% (In-Stat/MDR), image sensors have become a significant silicon technology driver.

Charge-coupled devices (CCDs) have traditionally been the dominant image-sensor technology. Recent advances in the design of image sensors implemented in complementary metal-oxide semiconductor (CMOS) technologies have led to their adoption in several high-volume products, such as the optical mouse, PC cameras, mobile phones, and high-end digital cameras, making them a viable alternative to CCDs. Additionally, by exploiting the ability to integrate sensing with analog and digital processing down to the pixel level, new types of CMOS imaging devices are being created for man-machine interface, surveillance and monitoring, machine vision, and biological testing, among other applications.

In this article, we provide a basic introduction to CMOS image-sensor technology, design, and performance limits and present recent

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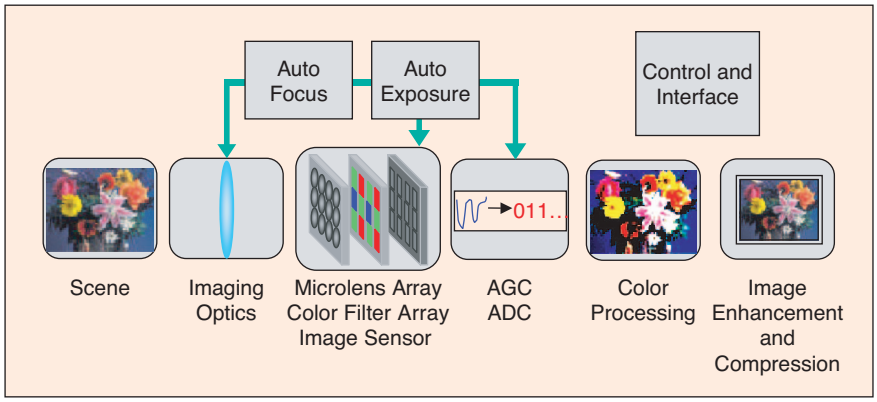
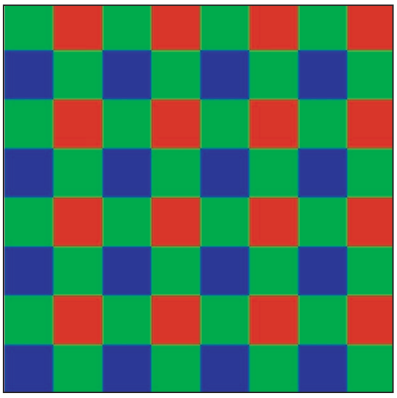
developments and future directions in this area. We begin with a brief description of a typical digital imaging system pipeline. We also discuss image-sensor operation and describe the most popular CMOS image-sensor architectures. We note the main non-idealities that limit CMOS image sensor performance, and specify several key performance measures. One of the most important advantages of CMOS image sensors over CCDs is the ability to integrate sensing with analog and digital processing down to the pixel level. Finally, we focus on recent developments and future research directions that are enabled by pixel-level processing, the applications of which promise to further improve CMOS image sensor performance and broaden their applicability beyond current markets.



1. The imaging system pipeline.

IMAGING SYSTEM PIPELINE

An image sensor is one of the main building blocks in a digital imaging system such as a digital still or video camera. Figure 1 depicts a simplified block diagram of an imaging-system architecture. First, the scene is focused on the image sensor using the imaging optics. An image sensor comprising a two-dimensional array of pixels converts the light incident at its surface into an array of electrical signals. To perform color imaging, a color-filter-array (CFA) is typically deposited in a certain pattern on top of the image sensor pixel array (see Figure 2 for a typical red-green-green-blue Bayer CFA). Using such a filter, each pixel produces a signal corresponding to only one of the three colors, e.g., red, green, or blue. The analog pixel data (i.e., the electrical signals) are read out of the image sensor and digitized by an analog-to-digital converter (ADC). To produce a full color image, i.e., one with red, green and blue color values for each pixel, a spatial interpolation operation known as *demosaicking* is used. Further digital-signal processing is used to perform white balancing and color correction as well as to diminish the adverse effects of faulty pixels and imperfect optics. Finally, the image is compressed and stored in memory. Other processing and control operations are also included for performing auto-focus, auto-exposure, and general camera control.



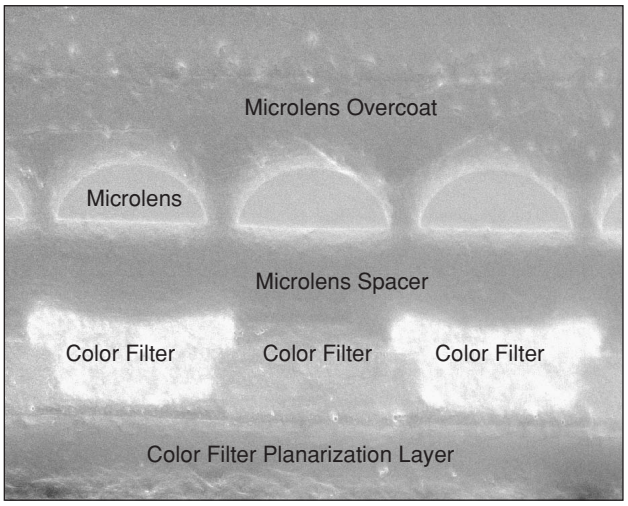
2. The color filter array Bayer pattern.

Each component of an imaging system plays a role in determining its overall performance. Simulations [1] and experience, however, show that it is the image sensor that often sets the ultimate performance limit. As a result, there has been much work on improving image sensor performance through technology and architecture enhancements as discussed in subsequent sections.

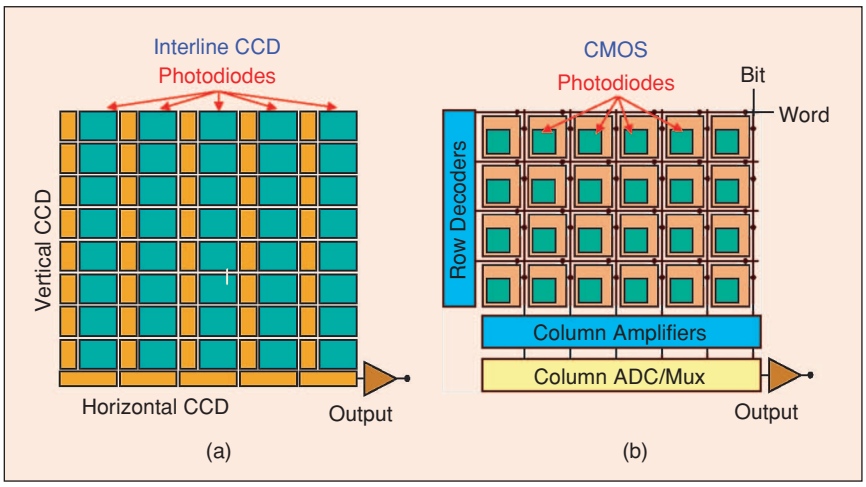
IMAGE-SENSOR ARCHITECTURES

An area image sensor consists of an array of pixels, each containing a photodetector that converts incident light into photocurrent and some of the readout circuits needed to convert the photocurrent into electric charge or voltage and to read it off the array. The percentage of area occupied by the photodetector in a pixel is known as *fill factor*. The rest of the readout circuits are located at the periphery of the array and are multiplexed by the pixels. Array sizes can be as large as tens of megapixels for high-end applications, while individual pixel sizes can be as small 2×2 μm. A microlens array is typically deposited on top of the pixel array to increase the amount of light incident on each photodetector. Figure 3 is a scanning electron microscope (SEM) photograph of a CMOS image sensor showing the color filter and microlens layers on top of the pixel array.

The earliest solid-state image sensors were the bipolar and MOS photodiode arrays developed by Westinghouse, IBM, Plessy, and Fairchild in the late 1960s [2]. Invented in 1970 as an analog memory device, CCDs quickly became the dominant image sensor technology. Although several MOS image sensors were reported in the early 1980s, today's CMOS image sensors are based on work done starting around the mid 1980s at VLSI Vision Ltd and the Jet Propulsion Laboratory. Up until the early 1990s, the passive pixel sensor (PPS) was the CMOS image sensor technology of choice [3]. The feature sizes of the available CMOS technologies were too large to accommodate more than the single transistor and three interconnect lines in a PPS pixel. PPS devices, however, had much lower performance than CCDs, which limited their applicability to low-end machine-vision applications. In the early 1990s, work began on the modern CMOS active pixel sensor (APS), conceived originally in 1968 [4], [5]. It was quickly realized that adding an amplifier to each pixel significantly increases sensor speed and improves its signal-to-noise ratio (SNR), thus overcoming the shortcomings of PPS. CMOS technology feature sizes,



3. A cross-section SEM photograph of an image sensor showing the microlens and CFA deposited on top of the photodetectors.



4. (a) Readout architectures of interline transfer CCD and (b) CMOS image sensors.

however, were still too large to make APS commercially viable. With the advent of deep submicron CMOS and integrated microlens technologies, APS has made CMOS image sensors a viable alternative to CCDs. Taking further advantage of technology scaling, the digital pixel sensor (DPS), first reported in [6], integrates an ADC at each pixel. The massively parallel conversion and digital readout provide very high speed readout, enabling new applications such as wider dynamic range (DR) imaging, which is discussed later in this article.

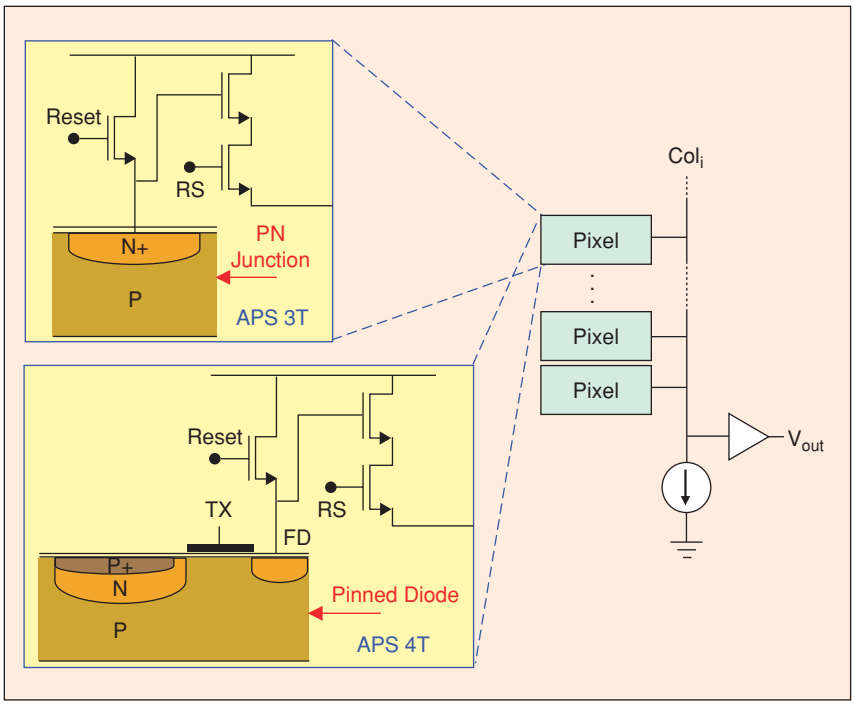
Many of the differences between CCD and CMOS image sensors arise from differences in their readout architectures. In a CCD [see Figure 4(a)], charge is shifted out of the array via vertical and horizontal CCDs, converted into voltage via a simple follower amplifier, and then serially read out. In a CMOS image sensor, charge voltage signals are read out one row at a time in a manner similar to a random access memory using row and column select circuits [see Figure 4(b)]. Each readout architecture has its advantages and disadvantages. The main advantage of the CCD readout architecture is that it requires minimal pixel overhead, making it possible to design image sensors with very small pixel sizes. Another important advantage is that charge transfer is passive and therefore does not introduce temporal noise or pixel to pixel variations due to device mismatches, known as fixed-pattern noise (FPN). The readout path in a CMOS image sensor, by comparison, comprises several active devices that introduce both temporal noise and FPN. Charge transfer readout, however, is serial resulting in limited readout speed. It is also high power due to the need for high-rate, high-voltage clocks to achieve near-perfect charge transfer efficiency. By comparison, the random access readout of CMOS image sensors provides the potential for high-speed readout and window-of-interest operations at low power consumption. There are several recent examples of CMOS image sensors operating at hundreds of frames per second with megapixel or more resolution [7]–[9]. The high-speed readout also makes CMOS image sensors ideally suited for implementing very high-resolution imagers with multi-megapixel resolutions, especially for video applications. Recent examples of such high-resolution CMOS imagers include the 11-megapixel sensor used in the Canon EOS-1 camera and the 14-megapixel sensor used in the Kodak DCS camera.

Other differences between CCDs and CMOS image sensors arise from differences in their fabrication technologies. CCDs are fabricated in specialized technologies solely optimized for imaging and charge transfer. Control over the fabrication technology also makes it possible to scale pixel size down without significant degradation in performance. The disadvantage of using such specialized technologies, however, is the inability to integrate other camera functions on the same chip with the sensor. CMOS image sensors, on the other hand, are fabricated in mostly standard technologies and thus can be readily integrated with other analog and digital processing and control circuits. Such integration further reduces imaging system power and size and enables the implementation of new sensor functionalities, as will be discussed later.

Some of the CCD versus CMOS comparison points made here should become clearer as we discuss image sensor technology in more detail.

Photodetection

The most popular types of photodetectors used in image sensors are the reverse-biased positive-negative (PN) junction photodiode and the P+/N/P pinned diode (see Figure 5). The structure of the pinned diode provides improved photoresponsivity (typically with enhanced sensitivity at shorter wavelengths) relative to the standard PN junction [10]. Moreover, the pinned diode exhibits lower thermal noise due to the passivation of defect and surface states at the Si/SiO_2 interface, as

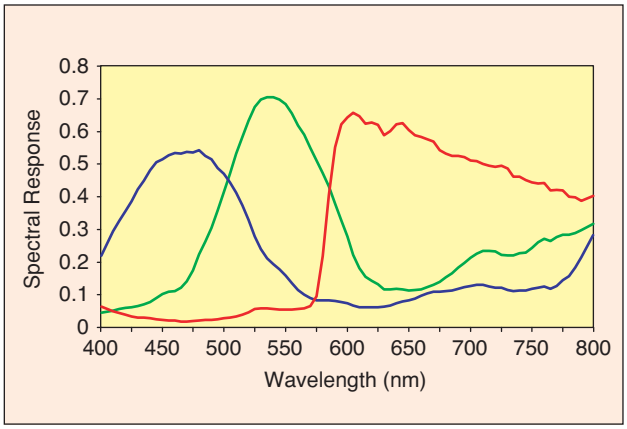


5. A schematic of a 3- and 4-T active pixel sensor (APS).

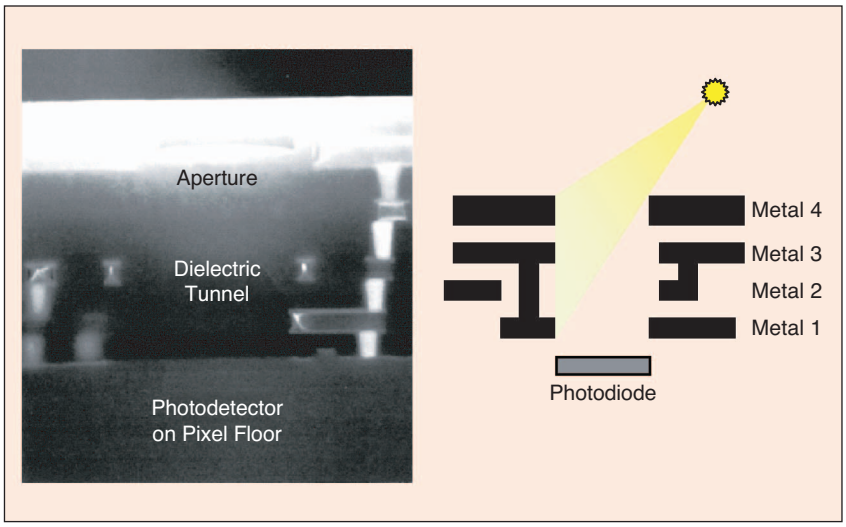
well as a customizable photodiode capacitance via the charge transfer operation through transistor TX. However, imagers incorporating pinned diodes are susceptible to incomplete charge transfer, especially at lower operating voltages causing ghosting artifacts to appear in video-rate applications.

The main imaging characteristics of a photodiode are *external quantum efficiency* (QE) and *dark current*. External QE is the fraction of incident photon flux that contributes to the photocurrent in a photodetector as a function of wavelength (typically in the 400–700 nm range of visible light). It is typically combined with the transmittance of each color filter to determine its overall spectral response. The spectral response for a typical CMOS color image sensor fabricated in a modified 0.18-μm process is shown in Figure 6. External QE can be expressed as the product of *internal QE* and *optical efficiency* (OE). Internal QE is the fraction of photons incident on the photodetector surface that contributes to the photocurrent. It is a function mainly of photodetector geometry and doping concentrations and is always less than one for the above silicon photodetectors. OE is the photon-to-photon efficiency from the pixel surface to the photodetector's surface. The geometric arrangement of the photodetector with respect to other elements of the pixel structure, i.e., shape and size of the aperture; length of the dielectric "tunnel"; and position, shape, and size of the photodetector, all determine OE. Figure 7 is an SEM photograph of a cross section through a CMOS image sensor pixel illustrating the tunnel through which light must travel before reaching the photodetector. Experimental evidence shows that OE can have a significant role in determining the resultant external QE [11].

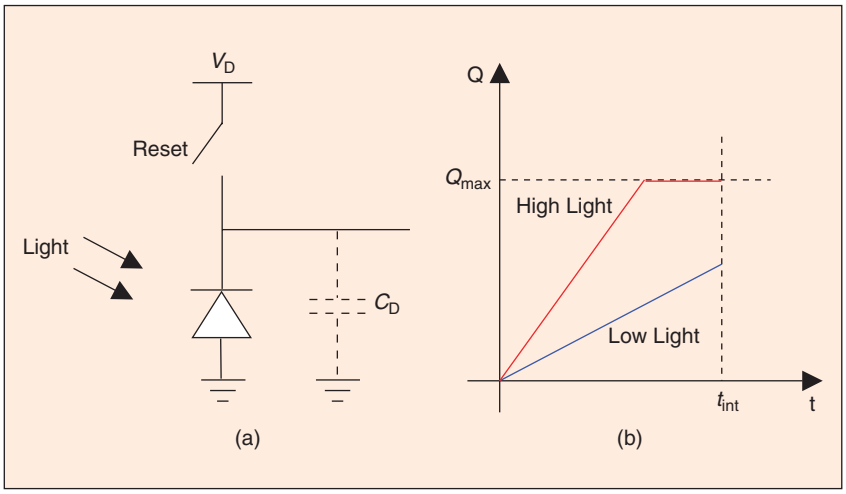
The second important imaging characteristic of a photodetector is its leakage or dark current. Dark current is the photodetector current when no illumination is present. It is generated by several sources, including carrier thermal generation and diffusion in the neutral bulk, thermal generation in the depletion region, thermal generation due to surface states at the silicon-silicon dioxide interface, and thermal generation due to interface traps (caused by defects) at the diode perimeter. As discussed in more detail later in this article, dark current is detrimental to imaging performance under low illumination as it



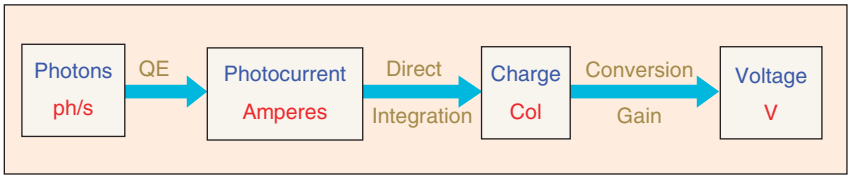
6. A spectral response curve for a typical 0.18-μm CMOS image sensor.



7. An illustration of optical "tunnel" above photodetector and pixel vignetting phenomenon.



8. (a) A schematic of pixel operating in direct integration. (b) Charge versus time for two photocurrent values.



9. A block diagram of signal path for an image sensor.

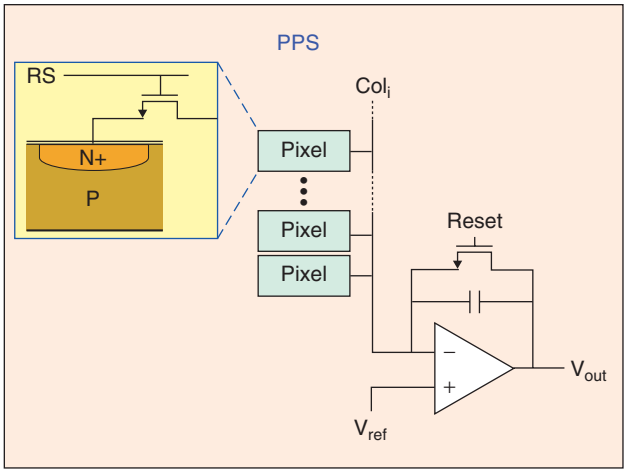
introduces shot noise that cannot be corrected for as well as nonuniformity due to its large variation over the sensor array. Much attention is paid to minimizing dark current in CCDs, which can be as low as 1–2 pA/cm^2, through the use of gettered, high-resistivity wafers to minimize traps from metallic contamination as well as buried channels and multiphase pinned operation to minimize surface generated dark current [12]. Dark current in standard submicron CMOS processes is orders of magnitude higher than in a CCD and several process modifications are used to reduce it [13]. Somewhat higher dark current can be tolerated in CMOS image sensors, since, in a CCD, dark current affects both photodetection and charge transfer.

As the range of photocurrents produced under typical illumination conditions is too low (in the range of femto- to picoamperes) to be read directly, it is typically integrated and read out as charge or voltage at the end of the exposure time. This operation, known as *direct integration*, is illustrated in Figure 8. The photodiode is first reset to a voltage V_D. The reset switch is then opened and the photocurrent i_{ph} as well as the dark current, i_{dc}, are integrated over the diode capacitance C_D. At the end of integration, the charge accumulated over the capacitance is either directly read out, as in CCDs or PPS, and then converted to voltage or directly converted to voltage and then read out as in APS. In both cases, the charge-to-voltage conversion is linear and the sensor *conversion gain* is measured in microvolts per electron. The charge versus time for two photocurrent values is illustrated in Figure 8(b). In the low light case, the charge at the end of integration is proportional to the light intensity, while in the high light case, the diode saturates, and the output charge is equal to the well capacity Q_{well}, which is defined as the maximum amount of charge (in electrons) that can be held by the integration capacitance.

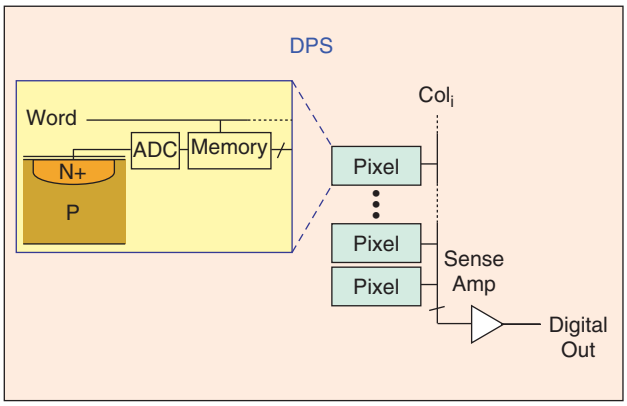
Figure 9 depicts the signal path for an image sensor from the incident photon flux to output voltage. This conversion is nearly linear and is governed by three main parameters; external QE, integration time (t_{int}), and conversion gain.

PPS, APS, and DPS Architectures

There are different flavors of CMOS image-sensor readout architectures. We describe PPS, which is the earliest CMOS image-sensor architecture (see Figure 10), the three and four transistor (3 and 4 T) per pixel APS, which are the most popular architectures at present (see Figure 5), and DPS (see Figure 11). The PPS pixel includes a photodiode and a row-select transistor. The readout is performed one row at a time in a staggered "rolling shutter" fashion. At the end of integration,



10. A schematic of a passive pixel sensor (PPS).



11. A schematic of a diagram pixel sensor (DPS).

charge is read out via the column charge-to-voltage amplifiers. The amplifiers and the photodiodes in the row are then reset before the next row readout commences. The main advantage of PPS is its small pixel size. The column readout, however, is slow and vulnerable to noise and disturbances. The APS and DPS architectures solve these problems, but at the cost of adding more transistors to each pixel.

> One of the most important advantages of CMOS image sensors over CCDs is the ability to integrate sensing with analog and digital processing down to the pixel level.

The 3-T APS pixel includes a reset transistor, a source follower transistor to isolate the sense node from the large column bus capacitance and a row select transistor. The current source component of the follower amplifier is shared by a column of pixels. Readout is performed one row at a time. Each row of pixels is reset after it is read out to the column capacitors via the row access transistors and column amplifiers. The 4-T APS architecture employs a pinned diode, which adds a transfer gate and a floating diffusion (FD) node to the basic 3-T APS pixel architecture. At the end of integration, the accumulated charge on the photodiode is transferred to the FD node. The transferred charge is then read out as voltage in the same manner as in the 3-T architecture. Note that, unlike CCD and PPS, APS readout is nondestructive.

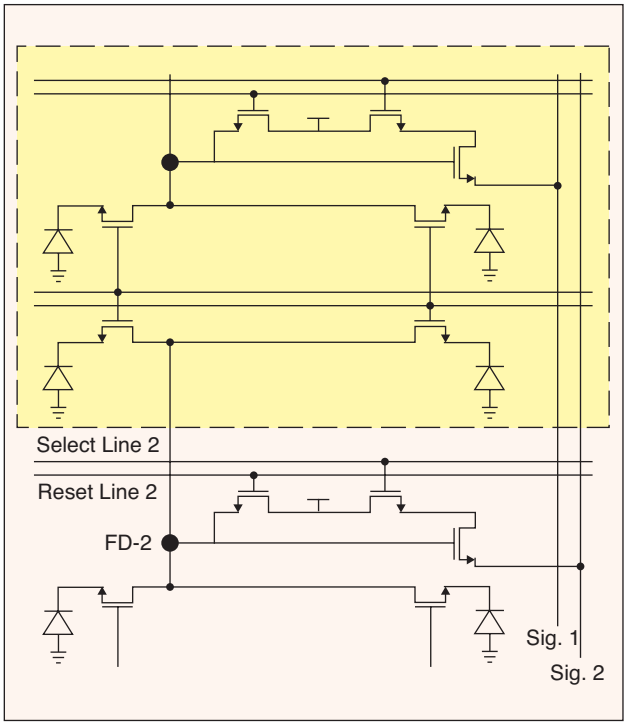
Although the main purpose of the extra transistors in the APS pixel is to provide signal buffering to improve sensor readout speed and SNR, they have been used to perform other useful functions. By appropriately setting the gate voltage of the reset transistor in an APS pixel, *blooming*, which is the overflow of charge from a saturated pixel into its neighboring pixels, can be mitigated [14]. The reset transistor can also be used to enhance DR via well capacity adjusting, as described in [15].

Each of the APS architectures has its advantages and disadvantages. A 4-T pixel is either larger or has a smaller fill factor than a 3-T pixel implemented in the same technology. On the other hand, the use of a transfer gate and the FD node in a 4-T pixel decouples the read and reset operations from the integration period, enabling true correlated double sampling (CDS), as will be discussed in detail later in this article. Moreover, in a 3-T pixel, conversion gain is set primarily by the photodiode capacitance, while in a 4-T pixel, the capacitance of the FD node can be selected independently of the photodiode size, allowing conversion gain to be optimized for the sensor application.

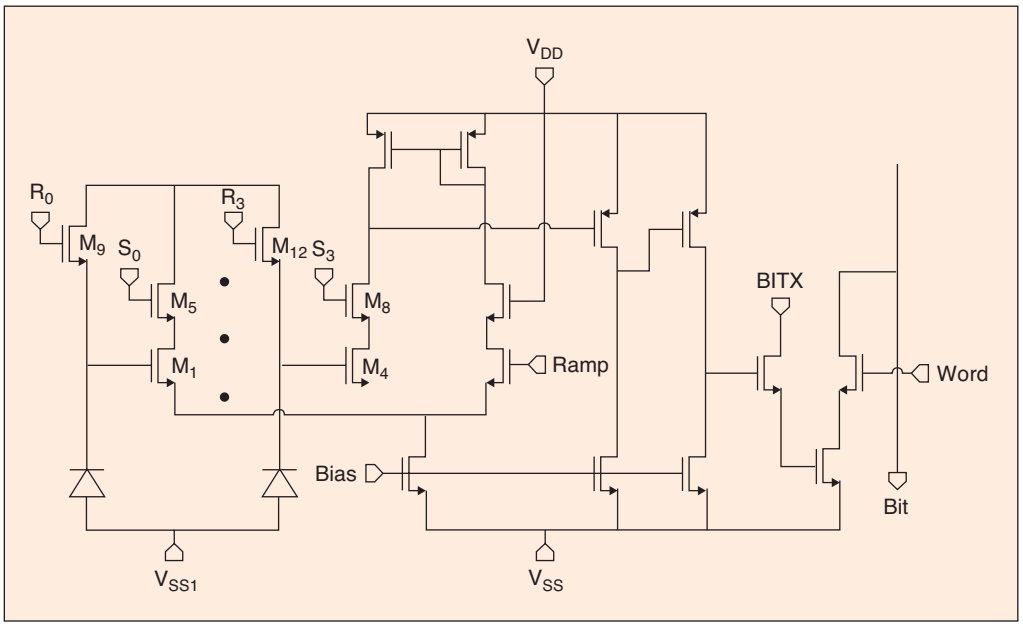
In applications such as mobile imaging, there is a need for small pixels to increase the spatial resolution without increasing the optical format (area of the sensor). CCDs have a clear advantage over CMOS image sensors in this respect due to their low pixel overhead and the use of dedicated technologies. To compete with CCDs, CMOS image sensor pixel sizes are being reduced by taking advantage of CMOS technology scaling and the process modifications discussed in the following section. In addition, novel pixel architectures that reduce the effective number of transistors per pixel by sharing some of the transistors among a group of neighboring pixels have been recently proposed [16], [17]. One example is the 1.75 T per pixel APS depicted in Figure 12 [16]. In this architecture, the buffer of the 4-T APS pixel is shared among each four neighboring pixels using the transfer gates as a multiplexer.

The third and most recently developed CMOS image sensor architecture is DPS, where analog-to-digital (A/D) conversion is performed locally at each pixel, and digital data is read out from the pixel array in a manner similar to a random access digital memory. Figure 11 depicts a simplified block diagram of a DPS pixel consisting of a photodetector, an ADC, and digital memory for temporary storage of data before digital readout via the bit-lines. DPS offers several advantages over analog image sensors, such as PPS and APS, including better scaling with CMOS technology due to reduced analog circuit performance demands and the elimination of read-related column FPN and column readout noise. More significantly, employing an ADC and memory at each pixel to enable massively parallel analot-to-digital conversion and high-speed digital readout, provides unlimited potential for high-speed "snap-shot" digital imaging.

The main drawback of DPS is that it requires the use of more transistors per pixel than conventional image sensors, resulting in larger pixel sizes or lower fill factors. However,



12. A pixel schematic of a 1.75-T/pixel APS.



13. An MCBS DPS pixel schematic.

since there is a lower bound on practical pixel size imposed by the wavelength of light, imaging optics, and DR, this problem becomes less severe as CMOS technology scales down to 0.18 μm and below.

As pixel size constraints make it infeasible to use existing ADC architectures, our group has developed several per-pixel ADC architectures that can be implemented with a small number of transistors per pixel. We have designed and prototyped three generations of DPS chips with different per-pixel ADC architectures. The first DPS chip comprised an array of 128 $\times$ 128 pixels with a first-order sigma-delta ADC shared within each group of 2 $\times$ 2 pixels and was implemented in 0.8-μm CMOS technology [6]. The sigma-delta technique can be implemented using simple circuits and is, thus, well suited to pixel-level implementation in advanced processes. However, since decimation must be performed outside the pixel array, too much data needs to be read out. The second generation of DPS solves this problem by using a Nyquist rate ADC approach [18]. The sensor comprised a 640 $\times$ 512 array of 10.5 $\times$ 10.5 μm pixels with a multichannel bit serial (MCBS) ADC shared within each group of 2 $\times$ 2 pixels and was implemented in 0.35 μm. A later 0.18-μm commercial implementation comprised a 742 $\times$ 554 array of 7 $\times$ 7 μm pixels [19]. Implementing an MCBS ADC only requires a 1-b comparator and a 1-b latch per each group of four pixels, as shown in Figure 13. Data from the array are read out one quad bit plane at a time, and the pixel values are assembled outside the array. Our most recent design utilized a standard digital 0.18-μm CMOS technology to integrate both a single-slope bit parallel ADC and an 8-b dynamic memory inside each pixel [9]. The chip comprised an array of 288 $\times$ 352 pixels and was the first image sensor to achieve a continuous throughput of 10,000 frames per second or one gigapixel per second. The digitized pixel data is read out over a 64-b wide bus operating at 167 MHz, i.e., over 1.3 GB/s. More specifically, each pixel contains a photodetector, a 1-b comparator, and eight 3-T memory cells in an area of 9.4 $\times$ 9.4 μm. Single-slope A/D conversion is performed simultaneously for all pixels via a globally distributed analog ramp and gray coded digital signals generated outside the array.

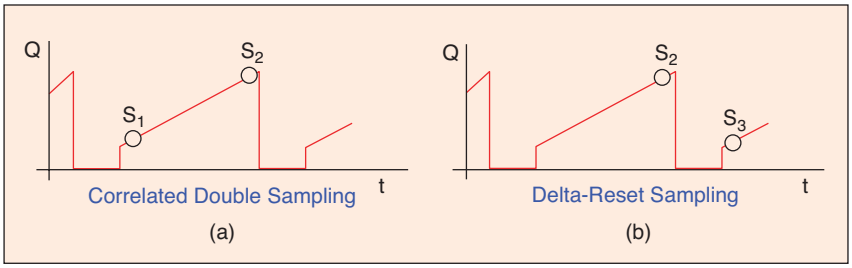
NONIDEALITIES AND PERFORMANCE MEASURES

Image sensors suffer from several fundamental and technology related nonidealities that limit their performance and effect image-sensor performance.

Temporal and Fixed Pattern Noise

Temporal noise is the most fundamental nonideality in an image sensor as it sets the ultimate limit on signal fidelity. This type of noise is independent across pixels and varies from frame to frame. Sources of temporal noise include photodetector shot noise, pixel reset circuit noise, readout circuit thermal and flicker noise, and quantization noise. There are more sources of readout noise in CMOS image sensors than CCDs introduced by the pixel and column active circuits.

In addition to temporal noise, image sensors also suffer from FPN, which is the pixel-to-pixel output variation under uniform illumination due to device and interconnect mismatches across the image sensor array. These variations cause two types of FPN: offset FPN, which is independent of pixel signal, and gain FPN or photo response nonuniformity (PRNU), which increases with signal level. Offset FPN is fixed



14. Sample times for CDS versus delta reset.

from frame to frame but varies from one sensor array to another. Again, there are more sources of FPN in CMOS image sensors than CCDs introduced by the active readout circuits. The most serious additional source of FPN is the column FPN introduced by the column amplifiers. Such FPN can cause visually objectionable streaks in the image.

Offset FPN caused by the readout devices can be reduced by CDS, as illustrated in Figure 14(a). Each pixel output is readout twice, once right after reset and a second time at the end of integration. The sample after reset is then subtracted from the one after integration. To understand the effect of this operation, we express the sampled noise at the end of integration as the sum of

1) integrated shot noise Q_{shot}
2) reset noise Q_{reset}
3) readout circuit noise Q_{read} due to readout device thermal and flicker (or $1/f$) noise
4) offset FPN due to device mismatches Q_{FPN}
5) offset FPN due to dark current variation, commonly referred to as dark signal nonuniformity (DSNU) Q_{DSNU}
6) gain FPN, commonly referred to as PRNU.

The output charge right after reset can thus be expressed as

$$S_1 = Q_{\text{reset}} + Q_{1,\text{read}} + Q_{\text{FPN}} \text{ electrons.}$$

After integration, the output charge is given by

$$S_2 = (i_{\text{ph}} + i_{\text{dc}})\, t_{\text{int}} + Q_{\text{shot}} + Q_{\text{reset}} + Q_{2,\text{read}} + Q_{\text{FPN}} + Q_{\text{DSNU}} + Q_{\text{PRNU}} \text{ electrons.}$$

Using CDS, the signal charge is estimated by

$$(S_2 - S_1) = (i_{\text{ph}} + i_{\text{dc}})\, t_{\text{int}} + Q_{\text{shot}} - Q_{1,\text{read}} + Q_{2,\text{read}} + Q_{\text{DSNU}} + Q_{\text{PRNU}} \text{ electrons.}$$

Thus, CDS suppresses offset FPN and reset noise but increases read noise power. This increase depends on how much CDS suppresses flicker noise; the shorter the time between the two samples, the more correlated their flicker noise components become and the more effective CDS is at suppressing flicker noise. CDS is particularly effective at suppression of flicker noise in charge-transfer devices. Specifically, CDS is performed on the floating-diffusion (FD) node directly without regard to the length of the integration period, since the FD node can be reset immediately before charge transfer. Note that CDS does not reduce DSNU. Since dark current in CMOS image sensors can be much higher than in CCDs, DSNU can greatly degrade CMOS image-sensor performance under low illumination levels. This is most pronounced at high temperatures, as dark current and, thus, DSNU exponentially increases with temperature, roughly doubling every 7 °C. DSNU can be corrected using digital calibration. However, strong dependence on temperature makes accurate calibration difficult. Although PRNU is also not reduced by performing CDS, its effect is usually not as detrimental since it affects sensor performance mainly under high illumination levels.

CDS can be readily implemented in the CCD and the 4-T APS architectures, but cannot be implemented in the 3-T APS architecture. Instead, an operation known as *delta-reset sampling* is implemented, whereby the pixel output is read after integration and then once again after the next reset. Since the reset noise added to the first sample is different from that added to the second, the difference between the two samples only suppresses offset FPN and flicker noise and doubles reset noise power [see Figure 14(b)].

SNR and DR

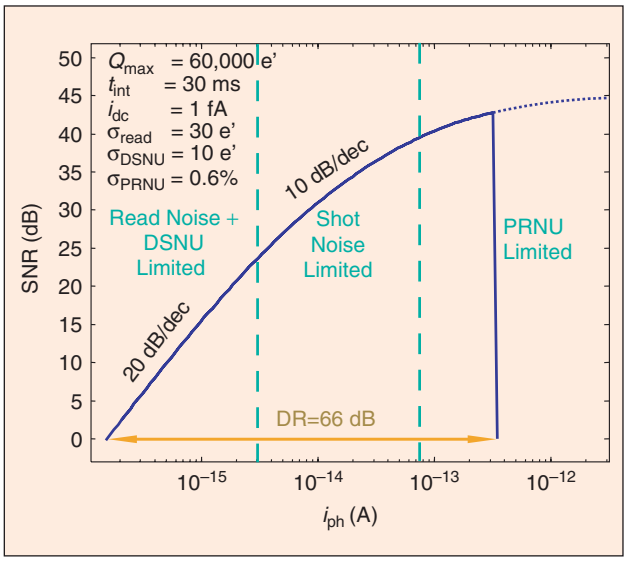
Temporal noise and FPN determine the range of illumination that can be detected by the image sensor, known as its DR, and the quality of the signals it produces within the detection range measured by the SNR.

Assuming CDS is performed and reset and offset FPN effectively cancelled, the noise power at the end of integration can be expressed as the sum of four independent components, shot noise with average power $\frac{1}{q}(i_{\text{ph}} + i_{\text{dc}})t_{\text{m}}$ electron^2, where q is the electron charge, read circuit noise due to the two readouts performed including quantization noise with average power σ^2_{read}, DSNU with average power σ^2_{DSNU} and PRNU with average power $\frac{1}{q^2}\,(\sigma_{\text{PRNU}}\, i_{\text{ph}}\, t_{\text{int}})^2$.

With this simplified noise model, we can quantify pixel signal fidelity using the SNR, which is the ratio of the signal power to the total average noise power, as

$$\text{SNR} = 10\log_{10} \times \frac{(i_{\text{ph}} t_{\text{int}})^2}{\left(q(i_{\text{ph}} + i_{\text{dc}})t_{\text{int}} + q^2\left(\sigma^2_{\text{read}} + \sigma^2_{\text{DSNU}}\right) + (\sigma_{\text{PRNU}}\, i_{\text{ph}}\, t_{\text{int}})^2\right)}.$$

SNR for a set of typical sensor parameters is plotted in Figure 15. Note that it increases with photocurrent, first at 20 dB per decade when readout noise and shot noise due to dark current dominate, then at 10 dB per decade when shot noise dominates, and then flattens out when PRNU is dominant, achieving a maximum roughly equal to the well capacity Q_{well} before saturation. SNR also increases with integration time.



15. SNR versus photocurrent (i_{ph}) for image sensor.

Thus, it is always preferred to have as long an integration time as possible. Sensor DR quantifies its ability to image scenes with wide spatial variations in illumination. It is defined as the ratio of a pixel's largest nonsaturating photocurrent $i_{\max}$ to its smallest detectable photocurrent $i_{\min}$. The largest saturating photocurrent is determined by the well capacity and integration time as $i_{\max} = qQ_{\text{well}}/t_{\text{int}} - i_{\text{dc}}$, while the smallest detectable signal is set by the root mean square (rms) of the noise under dark conditions.

Using our simplified sensor model, DR can be expressed as

$$DR = 20\log_{10}\frac{i_{\max}}{i_{\min}} = 20\log_{10}\frac{qQ_{\text{well}} - i_{\text{dc}}\,t_{\text{int}}}{\sqrt{qi_{\text{dc}}\,t_{\text{int}} + q^2\left(\sigma^2_{\text{read}} + \sigma^2_{\text{DSNU}}\right)}}.$$

Note that DR decreases as integration time increases due to the adverse effects of dark current. On the other hand, increasing well capacity, decreasing read noise, and decreasing DSNU increases sensor DR.

Spatial Resolution

Another important aspect of image-sensor performance is its spatial resolution. An image sensor is a spatial (as well as temporal) sampling device. As a result, its spatial resolution is governed by the Nyquist sampling theorem. Spatial frequencies in linepairs per millimeter (lp/mm) that are above the Nyquist rate cause aliasing and cannot be recovered. Below the Nyquist rate, low-pass filtering due to the optics, spatial integration of photocurrent, and crosstalk between pixels, cause the pixel response to fall off with spatial frequency. Spatial resolution below the Nyquist rate is measured by the modulation transfer function (MTF), which is the contrast in the output image as a function of frequency.

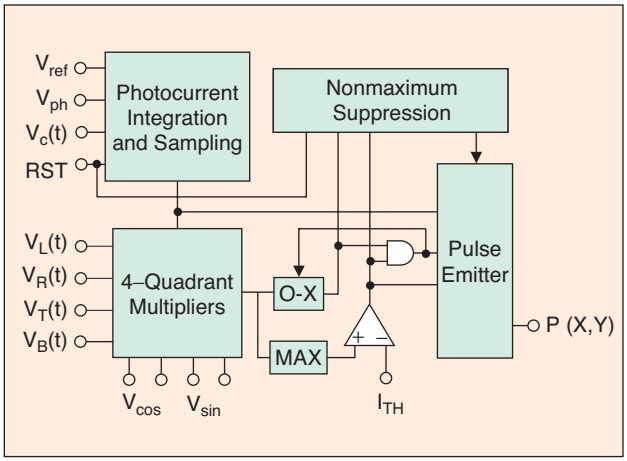
Technology Scaling Effects

CMOS image sensors benefit from technology scaling by reducing pixel size, increasing resolution, and integrating more analog and digital circuits on the same chip with the sensor. At 0.25 μm and below, however, a digital CMOS technology is not directly suitable for designing high-quality image sensors. The use of shallow junctions and high doping result in low photoresponsivity, and the use of shallow trench isolation (STI), thin gate oxide, and salicide result in unacceptably high dark current. Furthermore, in-pixel transistor leakage becomes a significant source of dark current. Indeed, in a standard process, dark current due to the reset transistor off-current and the follower transistor gate leakage current in an APS pixel can be orders of magnitude higher than the diode leakage itself.

To address these problems, there have been significant efforts to modify standard 0.18-μm CMOS technologies to improve their imaging performance. To improve photoresponsivity, nonsilicided deep junction diodes with optimized doping profiles are added to a standard process. To reduce dark current nonsilicided, double-diffused source/drain implantation as well as pinned diode structures are included. Hydrogen annealing is also used to reduce leakage by passivating defects [13]. To reduce transistor leakage, both the reset and follower transistors in an APS use thick gate oxide (70 Å). The reset transistor threshold is increased to reduce its off-current, while the follower transistor threshold is decreased to improve voltage swing.

Technology scaling also has detrimental effects on pixel OE. The use of silicon dioxide/nitride materials reduces light transmission to the photodetector. Moreover, as CMOS technology scales, the distance from the surface of the chip to the photodiode increases relative to the photodiode lateral dimension (see Figure 7). This is due to the reduction in pixel size and the fact that the thickness of the interconnect layers scales slower than the planar dimensions. As a result, light must travel through an increasingly deeper and/or narrower "tunnel" before reaching the photodiode surface. This is especially problematic for light incident at an oblique angle. In this case, the tunnel walls cast a shadow on the photodiode area. This phenomenon has been referred to as *pixel vignetting*, since it is similar to vignetting in optical systems. Pixel vignetting reduces the light incident at the correct photodiode surface, resulting both in a severe reduction in OE and in optical color crosstalk between adjacent pixels [20].

Several process modifications are being made in order to increase OE. Oxide materials with better light transmission properties are being used. Thinning of metal and oxide layers is used to decrease the aspect ratio of the tunnel above each photodetector, thereby reducing pixel vignetting. For example, in [17] a CMOS-based 1P2M process with 30% thinner metal and dielectric layers is developed and used to increase pixel sensitivity. Another technique for increasing OE is the placement of air gaps around each pixel in order to create a rudimentary optical waveguide whereby incident light at the surface is guided to the correct pixel below via total internal reflection. The air gaps also serve to significantly reduce optical spatial crosstalk, which can be particularly problematic as pixel sizes decrease [21].



16. A pixel block diagram of image extraction sensor [35].

INTEGRATION OF CAPTURE AND PROCESSING

The greatest promise of CMOS image sensor technology arises from the ability to flexibly integrate sensing and processing on the same chip to address the needs of different applications. As CMOS technology scales, it becomes increasingly feasible to integrate all basic camera functions onto a camera-on-chip [22], enabling applications requiring very small form-factor and ultra-low power consumption. Simply integrating blocks of an existing digital imaging system on a chip, however, does not fully exploit the potential of CMOS image sensor technology. With the flexibility to integrate processing down to the pixel level, the entire imaging system can be rearchitected to achieve much higher performance or to customize it to a particular application.

Pixel-level processing promises very significant advantages. This is perhaps best demonstrated by the wide adoption of APS over PPS and the subsequent development of DPS. In addition to adding more transistors to each pixel to enhance basic performance, there have been substantial efforts devoted to the development of computational sensors. These sensors promise significant reduction in system power by performing more sophisticated processing at the pixel level. By distributing and parallelizing the processing, speed is reduced to the point where analog circuits operating in subthreshold can be used. These circuits can perform complex computations while consuming very little power [23]. In the following subsection we provide a brief survey of this work.

Perhaps the most important advantage of pixel-level processing, however, is that signals can be processed in real time during integration. This enables several new applications, including high DR imaging, accurate optical-flow estimation, and three-dimensional (3-D) imaging. In many of these applications, the sensor output data rate can be too high, making multiple chip implementations costly, if not infeasible. Integrating frame buffer memory and digital-signal processing on the same chip with the sensor can solve this problem.

In this section, we will also briefly describe two related projects with which our group has been involved. The first project involves the use of vertical integration to design ultra high speed and high DR image sensors for tactical and industrial applications. The last subsection describes applications of CMOS image sensor technology to the development of lab-on-chips.

17. A high DR image synthesized from the low DR images shown in Figure 18.

18. Images of a high DR scene taken at exponentially increasing integration times.

This is a particularly exciting area, with many potential applications in medical diagnostics, pharmaceutical drug discovery, and biohazard detection. The work clearly illustrates the customization and integration benefits of CMOS image sensor technology.

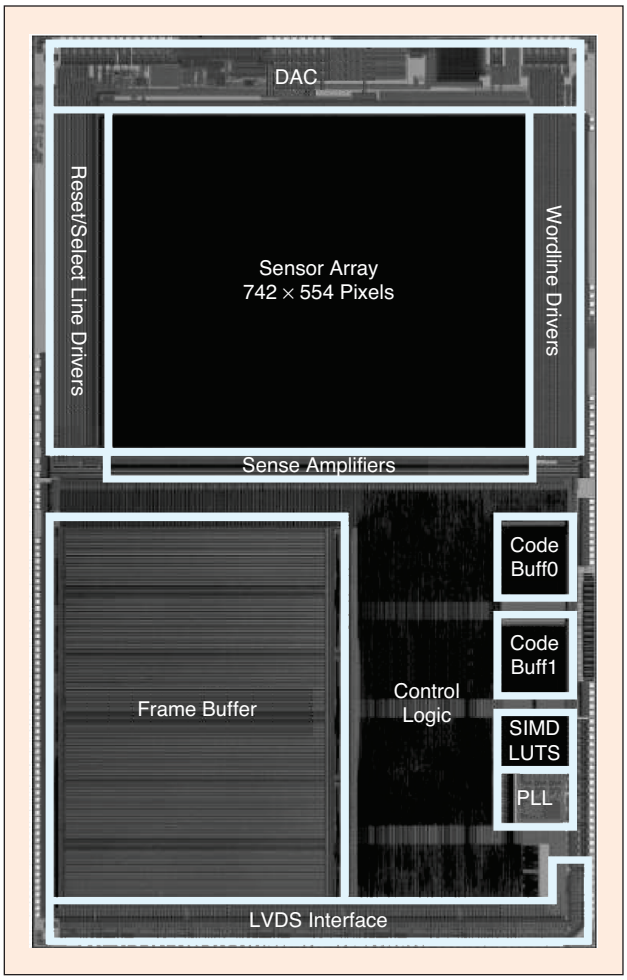
The ability to integrate sensing with processing is enabling a plethora of new imaging applications for the consumer, commercial, and industrial markets.

Computational Sensors

Computational sensors, sometimes referred to as neuromorphic sensors or silicon artificial retinas, are aimed mainly at machine-vision applications. Many authors have reported on sensors that derive optical motion flow vectors [24]–[28], which typically involve both local and global pixel calculations. Both temporal and spatial derivatives are locally computed. The derivatives are then used globally to calculate the coefficients of a line using least squares approximation. The coefficients of the line represent the final optical motion vector. The work on artificial silicon retinas [29]–[31] has focused on illumination-independent imaging and temporal low pass filtering, both of which involve only local pixel computations. Brajovic et al. [32] describe a computational sensor using both local and global interpixel processing that can perform histogram equalization, scene change detection, and image segmentation in addition to normal image capture. Rodriguez-Vazquez et al. [33] report on programmable computational sensors based on cellular nonlinear networks (CNN), which are well suited for the implementation of image-processing algorithms. Another approach, which is potentially more programmable, is the programmable artificial retina (PAR) described by Paillet et al. [34]. A PAR vision chip is a single instruction stream-multiple data stream (SIMD) array processor in which each pixel contains a photodetector, (possible) analog preprocessing circuitry, a thresholder, and a digital processing element. Although very inefficient for image capture, the PAR can perform a plethora of retinotopic operations including early vision functions, image segmentation, and pattern recognition. In [35], Ruedi describes a 120-dB DR sensor that can perform a variety of local pixel-level computations, such as for image contrast and orientation extraction. Each pixel communicates with its four neighboring pixels to compute the required spatial derivatives for contrast magnitude and direction extraction as well as to perform other image-processing functions, such as edge thinning via a nonmaximum suppression technique (see Figure 16). The chip consists of relatively large 69×69 μm^2 pixels comprising two multipliers, peak and zero crossing detectors, and a number of amplifiers and comparators.

High DR Sensors

Sensor DR is generally not wide enough to image scenes encountered even in everyday consumer photography. This is especially the case for CMOS image sensors, since their read noise and DSNU are typically larger than CCDs. For reference, standard CMOS image sensors have a DR of 40–60 dB, CCDs around 60–70 dB, while the human eye exceeds 90 dB by some measures. In contrast, natural scenes often exhibit greater than 100 dB of DR. To solve this problem, several DR extension techniques such as *well-capacity adjusting* [15], *multiple capture* [18], *time-to-saturation* [36], and *self-reset* [37] have been proposed. These techniques extend DR at the high illumination end, i.e., by increasing i_{max}. In multiple capture and time-to-saturation, this is achieved by adapting each pixel's integration time to its photocurrent value, while in self-reset the effective well capacity is increased by "recycling" the well. To perform these functions, most of these schemes require per-pixel processing. A comparative analysis of these schemes based primarily on SNR is presented in [38]–[40]. Here, we describe in some detail the multiple capture scheme.



19. A photomicrograph of color video system-on-chip.

Consider the high DR scene in Figure 17. Figure 18 shows a sequence of images taken at different integration times by a sensor whose DR is lower than the scene's. Note that none of these images contains all the details in the scene. The short integration time images contain the detail in the bright areas of the scenes but contain no detail in the dark areas due to noise, while long integration time images contain the details in the dark areas but none of the details in the bright areas due to saturation. Clearly, one can obtain a better "high DR" image of the scene by combining the details from these different integration time images, which can be done, for example, by using the *last sample before saturation* with proper scaling for each pixel (see Figure 17). The scheme involving capturing several images with different integration times and using them to assemble a high DR scheme is known as *multiple capture single image* [18].

> New types of CMOS imaging devices are being created for man-machine interface, surveillance and monitoring, machine vision, and biological testing, among other applications.

Dual capture has been used to enhance the DR for CCD sensors, CMD sensors [41], and CMOS APS sensors [42]. A scene is imaged twice, once using a short integration time and another using a much longer integration time, and the two images are combined into a high DR image. Two images, however, may not be sufficient to represent the areas of the scene that are too dark to be captured in the first image and too bright to be captured in the second. Also, it is preferred to capture all the images within a single normal integration time, instead of resetting and starting a new integration after each image. Capturing several images within a normal integration time, however, requires high-speed nondestructive readout, which CCDs cannot perform. DPS, on the other hand, can achieve very high-speed nondestructive readout and, therefore, can naturally implement the multiple capture scheme.

To implement multiple capture, high bandwidth between the sensor, memory, and processor is needed to perform the readouts and assemble the high DR image. By integrating the sensor with an on-chip frame buffer and digital-signal processing, such high bandwidth can be provided without unduly increasing clock speeds and power consumption. Using a modified 0.18-μm CMOS process, a recent paper [19] reported on a video system-on-chip that integrates a 742 $\times$ 554 DPS array, a microcontroller, an SIMD processor, and a full 4.9-Mb frame buffer (see Figure 19). The microcontroller and processor execute instructions relating to exposure time, region of interest, result storage, and sensor operation, while the frame buffer stores the intermediate samples used for reconstruction of the high DR image. The imaging system is completely programmable and can produce color video at a rate of 500 frames per second or standard frame rate video with over 100 dB of DR. Figure 20 shows a sample high DR scene imaged with the system and with a CCD.

The last sample before saturation method used to reconstruct a high DR image from multiple captures extends sensor DR only at the high illumination end. To extend DR at the low end, i.e., to reduce $i_{\min}$, one needs to reduce read noise and DSNU or increase integration time. Increasing integration time, however, is limited by motion blur and frame rate constraints. In [43], an algorithm is presented for extending DR at both the high and low illumination ends from multiple captures. The algorithm consists of two main procedures, photocurrent estimation and motion/saturation detection. Estimation is used to reduce read noise and thus enhance DR at the low illumination end. Saturation detection is used to enhance DR at the high illumination end, as previously discussed, while motion blur detection ensures that the estimation is not corrupted by motion. The algorithm operates completely locally. Each pixel's final value is computed recursively using only its captured values. The small storage and computation requirements of this algorithm make it well suited for single-chip implementation.

20. Comparison of CMOS DPS imager versus CCD imager using a HDR scene.

Video Rate Applications of High-Speed Readout

As discussed earlier, one of the main advantages of CMOS image sensors in general and DPS in particular is high frame rate readout. This capability can be used to enhance the performance of many image and video processing applications. The idea is to use the high frame-

rate capability to temporally oversample the scene and, thus, to obtain more accurate information about scene motion and illumination. This information is then used to improve the performance of image and standard frame-rate video applications. In the previous subsection, we discussed one important application of this general idea, which is DR extension via multiple capture. Another promising application of this idea is optical flow estimation (OFE), a technique used to derive an approximation for the motion field captured by a given video sequence. OFE is used in a wide variety of video-processing tasks such as video compression, 3-D surface structure estimation, super-resolution, motion-based segmentation, and image registration. In a recent paper [44], a method for obtaining high accuracy optical flow estimates at a conventional standard frame rate, e.g., ~30 frames per second, by first capturing and processing a high frame-rate version of the video is presented. The method uses the Lucas-Kanade algorithm (a gradient-based method) to obtain optical flow estimates at a high frame rate, which are then accumulated and refined to estimate the optical flow at the desired standard frame rate. It demonstrates significant improvements in optical flow estimation accuracy, both on synthetically generated video sequences and on a real video sequence captured using an experimental high-speed imaging system. The high-speed OFE algorithm requires small number of operations per pixel and can be readily implemented in a single chip imaging system similar to the one discussed in the previous section [45].

> CMOS image sensors are among the fastest growing and most exciting new segments of the semiconductor industry.

3-D Sensors

The extraction of the distance to an object at each point in a scene is referred to as 3-D imaging or depth sensing. Such depth images are useful for several computer vision applications such as tracking, object and face recognition, 3-D computer games, and scene classification and mapping. Various 3-D imagers employing a variety of techniques, such as triangulation, stereovision, or depth-from-focus, have been built; however, those based on light detection and ranging (LIDAR) have gained the most focus in recent years due to their relative mechanical simplicity and accuracy [46]. Time-of-flight (TOF) LIDAR-based sensors measure the time delay between an emitted light pulse, e.g., from a defocused laser, and its incoming reflection to calculate the depth map for a given scene. Niclass et al. [47] describe a sensor consisting of an array of avalanche diodes operating in Geiger mode that is sensitive and fast enough to perform photon counting and, consequently, TOF measurements. The high sensitivity allows for the use of a low-power illumination source, thereby reducing the intrusiveness of operating such a sensor in a normal environment. Another example is the Equinox sensor, an amplitude-modulated continuous wave LIDAR 3-D imager comprising a 64 × 64 array of pixels [48]. It derives a depth map by estimating the phase delay between an emitted modulated light source and the corresponding detected reflected signal. Each pixel includes two photogates: one switched in phase with the frequency of the emitted modulated light and the other switched completely out of phase. This alternation in the photogate voltage levels effectively multiplies the returning light signal by a square wave, hence approximating a pixel-level demodulation operation. This results in an estimate of the phase shift and, consequently, the depth at each pixel point in the image.

Vertically Integrated Sensor Arrays

Approaches that decouple sensing from readout and processing by employing a separate layer for photodetection are commonly used in infrared (IR) imaging sensors. In particular, many IR hybrid focal plane arrays use separately optimized photodetection and readout layers hybridized via indium bumps [49]. Such approaches are becoming increasingly attractive for visible-range imaging in response to the high transistor leakage and low supply voltages of deep submicron processes as well as a desire for increased integration. In [50], photoresponsivity is improved by using a deposited Si:H thin film on ASIC (TFA) layer for photodetection. In [51], it is shown that silicon-on-insulator (SOI) technology can provide for partial decoupling between readout and sensing. The handle wafer is used for photodetection with improved responsivity, especially at longer wavelengths, while the SOI-film is used for implementing the active readout circuitry with the buried oxide providing isolation between the two.

Taking this trend a step forward, vertically integrated sensor arrays, whereby multiple wafers are stacked and connected using through-wafer vias, promise even further performance gains. For example, in certain tactical, scientific, and industrial applications there is a need for imaging scenes with illumination/temperature ranges of 120 dB or more at speeds of 1,000 frames per second or more. These requirements far exceed the capability of current sensors, even using DR extension techniques such as multiple capture and well capacity adjusting. Other schemes can achieve higher DR than these two schemes but require significantly more per-pixel processing. Advances in vertical integration have significantly increased the amount of processing that can be integrated at each pixel, thus making the implementation of these high DR schemes more practical. In a recent paper [52], we described a high DR readout architecture, which we refer to as *folded multiple capture*. This architecture combines aspects from the multiple capture scheme with synchronous self-reset [53] to achieve over 120 dB of DR at 1,000 frames per second with high signal fidelity and low power consumption using simple robust circuits.

Lab on Chip

Current research in biotechnology has focused on increased miniaturization of biological handling and testing systems for increased speed/throughput, decreased reagent cost, and increased sensitivity. In addition, since most mainstream biological analyses are based on optical testing methods, such as fluorometry, luminometry, or absorptiometry, the use of CMOS-based image sensors for biological applications offers a clear advantage over other choices due to the ease of customizability, high integration, and low-cost of CMOS technology. Moreover, integration of such CMOS-based photodetectors with microfabricated microelectromechanical system (MEMS) substrates for reagent handling enables portable bioanalytical platforms for applications such as quantitative PCR, DNA sequencing, and pathogen detection. In [54], a 320×320 pixel CMOS-based lab-on-chip that performs cell manipulation is described. The chip is able to arbitrarily move electrically neutral particles via an applied electric field using an array of electrodes as well as simultaneously image the particles using an embedded APS array. Our group has built an 8×16 luminescence detection lab-on-chip fabricated in an optimized CMOS imaging process [55]. The integrated system is able to detect luminescence signals of below 10^{-6} lux at room temperature, enabling low-cost, portable DNA sequencing and pathogen detection. This high sensitivity is achieved through the use of low dark-current P+/N/Psub diodes, low-noise fully differential circuitry, high-resolution A/D conversion, and on-chip signal processing.

CONCLUSION

CMOS image sensors are among the fastest growing and most exciting new segments of the semiconductor industry. After a decade of research and development, CMOS image sensors have become one of the main silicon technology drivers, with tens of millions of parts shipped per year and a compound annual growth rate of over 28%. In addition, the ability to integrate sensing with processing is enabling a plethora of new imaging applications for the consumer, commercial, and industrial markets.

In this article, we provided an introduction to CMOS image sensor design and operation and discussed their limitations and performance measures. We discussed several recent developments that have substantially improved CMOS image sensor imaging quality and functionality, thus broadening their applicability to new large markets such as mobile imaging, digital still cameras, and security.

In spite of the significant advances in CMOS image-sensor technology and design, the smaller pixel size and generally better low-light performance of CCDs remain as the main obstacles toward their general adoption. We expect that further scaling of CMOS image sensor technology and improvements in their imaging performance will eventually erase any remaining advantage of CCDs. More importantly, we expect that many new and very large markets for imaging devices will be created by further exploitation of the integration of sensing and processing.

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